REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of August 14, 2002, has been received and contents carefully reviewed.

Claims 33-66 and 68-71 are currently pending in this application. Reconsideration and reexamination of this application is respectfully requested.

The Examiner has made a requirement for a new title. Applicant submits that the title is clearly indicative of the invention, however, to further prosecution of this application a new title is submitted herewith.

The Examiner rejected claims 33-47, 64-66, and 68-71 under 35 USC § 103(a) as being unpatentable over Applicant's Prior Art Figures (hereinafter "APAF") in view of Hebiguchi (US Patent No. 6,091,473). Applicant respectfully traverses this rejection.

Claim 33 is allowable at least for the reason that claim 33 recites a combination of elements including data and common electrodes parallel to the data bus line in the pixel region, the data and common electrodes having portions for first and second storage capacitors; a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlapping the gate and data bus lines; and a first alignment layer on the common electrode.

Claim 64 is allowable at least for the reason that claim 64 recites a combination of elements including data and common electrodes parallel to the data bus line in the pixel region; a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode; a light shielding layer on the passivation layer; and a first alignment layer on the common electrode.

Claim 69 is allowable at least for the reason that claim 64 recites a combination of

elements including data and common electrodes parallel to the data bus line in the pixel region; a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlaps the gate and data bus lines; a light shielding layer on the passivation layer; and a first alignment layer on the common electrode.

None of the cited references, singly or in combination, teaches or suggests at least these features of the claims.

In APAF, the first alignment layer 23a is formed on passivation layer 20. It does not appear that Hebiguchi even teaches an alignment layer. None of the cited references teach a first alignment layer on the common electrode as recited by claims 33, 64, and 69.

Hebiguchi does not teach or suggest the claimed invention as a whole. *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983); see also *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976). The invention of this application comprises an IPS liquid crystal display device having a common electrode on a passivation layer and a first alignment layer on the common electrode. Hebiguchi may teach a common electrode on a passivation layer, but fails to teach or suggest explicitly or implicitly a common electrode and a first alignment layer as recited by claims 33, 64, and 69.

Hebiguchi is not attempting to solve similar problems with the same solution. "[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole', which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103." *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). However, "discovery of the cause of a problem . . . does not always result in a patentable

invention. . . . [A] different situation exists where the solution is obvious from prior art which contains the same solution for a similar problem." *In re Wiseman*, 596 F.2d 1019, 1022, 201 USPQ 658, 661 (CCPA 1979) (emphasis in original).

Furthermore, the Examiner has not pointed out a particular finding as to the specific understanding or principle within the knowledge of a skilled artisan, either expressly or by implication that would have motivated one with no knowledge to combine or modify APAF. Applicant respectfully submits that no proper motivation or suggestion is found for one of ordinary skill in the art to modify APAF to arrive at the claimed device. Further, such combination is suggested only by the claimed invention, which is considered impermissible hindsight reconstruction. Through the combination of references used by the Examiner, he has taken a specific aspect of the claim, i.e., a common electrode, to be the only advantage of the invention, and disregarded the other elements of the claim. Accordingly, Applicant respectfully requests withdrawal of the rejection based on the combination of references. Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness. Applicant respectfully requests that the rejection under 35 USC § 103(a) be withdrawn.

Applicants submit that there is no motivation to combine these two references. Applicants submit that claims 33, 64, and 69 are allowable over the cited references.

Moreover, claims 34-47, 65-68, 70, and 71 are allowable by virtue of their dependence on claims 33, 64, and 69, which are believed to be allowable.

The Examiner rejected claims 48-60, 62, and 63 under 35 USC § 103(a) as being unpatentable over Applicant's Prior Art Figures (hereinafter "APAF") in view of Hebiguchi (US Patent No. 6,137,557). Applicant respectfully traverses this rejection.

Claim 48 is allowable at least for the reason that claim 48 recites a combination of elements including data and common electrodes parallel to the data bus line in the pixel region,

wherein the common electrode has first and second oblique sides; a passivation layer over the thin film transistor and the data electrode; and a first alignment layer on the common electrode.

None of the cited references teaches or suggests at least these features of the claims. As discussed above, the combination of APAF and Hebiguchi ('473) does not teach or suggest a first alignment layer on the common electrode. Hebiguchi ('557) fails to cure the deficiencies of APAF and Hebiguchi ('473). Applicants submit that claim 48 is allowable over the cited references. Applicant respectfully requests that the rejection under 35 USC § 103(a) be withdrawn.

Moreover, claims 49-60 62, and 63 are allowable by virtue of their dependence on claim 48, which is believed to be allowable.

The Examiner rejected claim 61 under 35 USC § 103(a) as being unpatentable over Applicant's Prior Art Figures (hereinafter "APAF") in view of Hebiguchi (US Patent No. 6,137,557) and Hebiguchi (US Patent No. 6,091,473). Applicant respectfully traverses this rejection.

As discussed above, the combination of APAF and Hebiguchi ('557) does not teach or suggest a first alignment layer on the common electrode. Hebiguchi ('473) fails to cure the deficiencies of APAF and Hebiguchi ('557). Applicants submit that claim 61 is allowable over the cited references. Applicant respectfully requests that the rejection under 35 USC § 103(a) be withdrawn.

The Examiner objected to claim 67 as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to**

show changes made."

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7371.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By 

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Version With Markings to Show Changes Made

Please amend the claims as follows:

33. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, the data and common electrodes having portions for first and second storage capacitors;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlapping the gate and data bus lines; and

a first alignment layer [over] <u>on</u> the common electrode.

48. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, wherein the

common electrode has first and second oblique sides;

a passivation layer over the thin film transistor and the data electrode; and

a first alignment layer [over] on the common electrode.

64. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode;

a light shielding layer on the passivation layer; and

a first alignment layer [over] on the common electrode.

69. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the

common electrode is formed on the passivation layer parallel to the data electrode and overlaps the gate and data bus lines;

a light shielding layer on the passivation layer; and

a first alignment layer [over] <u>on</u> the common electrode.